Next Generation PCIe Network Fabric for Simulators and Performance Computing

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ABSTRACT

Simulator use cases are pushing the limits of the current technology in network fabrics with regard to bandwidth and latency across their infrastructure deployments. Many leading technology companies (HP, Intel) have suggested that the network is the bottleneck for performance and that a new network fabric for the compute environment can help solve performance barriers for these technology implementations. Intel has further discussed RSD(Rack Scale Design) (Intel, 2018, p. 1) as a way of making simulator and compute environments more aligned with the workloads on them by disaggregating and re-aggregating compute, memory, storage, accelerators (GPUs - Graphics Processing Unit, FPGAs - Field Programmable Gate Arrays), and networking into more efficient stacks.

New patented PCIe (Peripheral Component Interconnect express - industry standard) based network fabric has recently been used to implement this methodology to solve the bandwidth and latency issues by allowing PCIe to extend throughout the datacenter or simulator cluster. This new capability provides disruptive technology gains for high performance computing and is being considered for deployment in High Performance Computer Centers throughout the DoD. Applying this technology to simulator and training use cases will offer new gains in latency (minimum of 10x less), provide for support of legacy environments at lower costs and support near theoretical bandwidth performance needed to support new technology programs such as STE (Synthetic Training Environment), NCRC (National Cyber Range Complex), and PCTE (Persistent Cyber Training Environment).

This abstract will outline some of the gains we have seen implementing this technology and show how it can be implemented in the simulator world. This new technology will drastically change the architecture implementations, decrease costs and increase performance for these environments across a wide range of use cases in the IITSEC community.

ABOUT THE AUTHORS

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HIGH PERFORMANCE SIMULATION (HPS): A CHANGING AND CHALLENGING DATA DRIVEN ENVIRONMENT

The exponential increases in the amount of data being collected, and that must be analyzed and stored, and then drive simulations is driving the rapid adoption of advanced big data analytics and Artificial Intelligence (AI) (Kenneally, Hoppe, 2018, p. 14-16) which is challenging the fundamental architectures of today's HPS data centers and endpoints, in a way not seen since the 1990s.

AI, and the associated Machine Learning (ML) and Deep Learning (DL) applications are fueling demand for fundamental change in the creation of compute and storage clusters. Faster and larger storage arrays, and a rapid proliferation of specialized compute accelerators, like GPUs, FPGAs and custom ASICs, are creating bottlenecks and configuration problems for the interconnect systems, as the traditional networks were never designed to handle the performance requirements of these simulation workloads and devices.

Further, the rapid pace of change in acceleration technology and AI software fuels the need for flexible and easy to upgrade architectures, capable of incorporating new technology without demanding forklift upgrades to expensive equipment. This means disaggregating elements of the traditional server into separate pieces that can be easily shared and aggregated for different workloads (Kenneally, Hoppe, 2018, p. 15). But, in order to effectively disaggregate and aggregate, storage and accelerators, the interconnects must support both an exceptionally low latency and high bandwidth.

Owners and administrators are being pressured by end users to lower barriers of adoption and in turn automate the complex administration activities within the HPS environment. Admin support for open source tool automation, delivering easy to use self-service portals and allowing HPS users to perform build on-demand composable HPS infrastructure is needed to support DevOps for simulation environments, large scale simulation and training exercises and experiments.

And, of course, HPS data center managers want to drive high utilization of expensive new storage and acceleration products and support legacy infrastructure to keep both Capex and Opex costs down as referenced by studies and guidelines from the EU (Acton, Bertoldi, Booth, Flucker, Newcombe, Royer, Tozer, 2018, p. 3).

Add all these up, and these Advanced Scale Computing, Enterprise, Cloud and Edge, and Simulation/Training centers need both scale-up and then scale-out resources across clusters and require a network technology that will grow in both directions in order to support programs like PCTE (Persistent Cyber Training Environment) and STE (Synthetic Training Environment).

Two potential solutions both raise new issues. Scaling-up computing systems into ever-larger "super-servers" is generally cost prohibitive for all but the largest academic or government institutions. Scaling-out computer power by replicating servers introduces overprovisioning and underutilization inefficiencies.

A few IT technology industry efforts are aimed at overcoming these issues:

- Numerous companies—from established to startup—are developing a new wave of more efficient application specific accelerators. Rather than general purpose GPUs, these chips work faster and use less power because they are designed for very specific processing tasks.
- SSD (Solid State Disk) storage providers are rapidly improving performance.
- Advanced Scale Computing (ASC) is disaggregating resources into a composable infrastructure where compute, storage and accelerator resources can be accessed on-demand.

But, while disaggregating resources is the right solution, now the system interconnect that enables composability becomes crucial. Insufficient speed and high latency in the interconnect networks create bottlenecks in scaling-up and scaling-out with ASC for HPS environments (Kenneally, Hoppe, 2018, p. 14-15). The underlying question for consumers of the infrastructure then becomes: how can one best manage all these new compute, storage, and network resources to break the constraints of prepacked servers and scale computing to meet heavy demands of simulation environments, while not exceeding the budget constraints?

SOLUTIONS FOR HIGH PERFORMANCE SIMULATION ENVIRONMENTS

High Performance PCIe Based Interconnect Network

Starting with a fundamentally different architecture, a PCIe interconnect network eliminates the network bottleneck associated with networking. This PCIe network architecture can construct a multi-rack, composable infrastructure that performs as if every storage and compute element were inside a single box, providing many benefits:

- Native PCI Express (PCIe) communication between hundreds of mixed processing units, cutting latency by eliminating the entire translation layer required by other interconnect network options.
- True Direct Memory Access and sharing of all connected processors and memory with point-to-point connections between any two devices, reducing customer investment in these resources.
- Dynamically disaggregation and composable, scalable, and elastic infrastructure.
- A roadmap for end-to-end data speed improvements across the entire interconnect network.
- Legacy support for HPS resources (PCIe version 1,2)
- Support for generic compute and storage devices (Intel, AMD, ARM, Nvidia, WDC, etc.)

Composable Infrastructure HPS Environment

As referenced by Intel about Rack Scale Design (Intel, 2018, p. 1-2) and HPE (Lowe, 2016, 23-24) about the advantages of composing infrastructure resources, allows for the infrastructure to match the simulation workload rather than current methodologies where the simulation workload is made to match the infrastructure. By changing this methodology, simulation developers will be free to incorporate more complex AI based technologies and not be constrained by the fixed infrastructure architectures which can limit performance and capability for complex simulations.

Self Service Portal for Provisioning Composable HPS Infrastructure

Many entities today are struggling with how to efficiently manage their HPS infrastructure with the continuous pressure to reduce cost while increasing performance, capacity, and ease of use for their consumers. These entities have identified the following infrastructure management needs (Reynolds, Campbell, 2019, p.107-108):

- Support of new technologies
    - New Interconnect for networking based on PCIe resources
- Scheduling, reserving, managing, deploying (lifecycle) environments
- Scaling
- Auto provisioning of resources (physical and virtual)
- Supporting converged infrastructure and legacy hardware
    - Support of cross domains (public and private clouds)

- Automation Framework to control provisioning from PCIe thru Layer 7
- IT admin activities
    - Auto-discovery, lab resets, resource health-checks for simulation resources
    - Powering down devices when not in use
    - Support for maintenance modes on resources
    - Integrating Help Desk applications into the workflow of administration of the HPS Environment
    - Spinning up new resources on demand for scaling support, etc.
    - Adding workload provisioning on top of the compute stack optimization of the provisioning and orchestration specific to the stack and the workload
- Supporting multiple tenancies and domains and geographic locations
- Configuration management of HPS resources
- Enabling user automation (configuring and deploying workloads, Virtual machines, containers, DevOps flows, sandboxing, etc.)
- Sharing of intellectual property
- Support processes (DevOps, DevSecOps, test, etc.), automation, configurations, resources, use cases, etc.
- Integration with other tools such Help Desk, Ticketing systems, and Simulators
- Metrics on the processes/activities, resources, usage, and users, to manage the lifecycle of the environment

This list is by no means complete, but it does address the majority of the problems seen by these entities. All of the above actions need to be handled in a standardized and centralized approach in order to be effective and consumable by the different roles involving the use of the HPS infrastructure. The actions need to be managed with a lifecycle approach for both the management of the HPS infrastructure and the activities in the HPS environment. The maintenance of resources, the roll back of configurations, and the validation testing of an environment before releasing it to the consumers are all examples of actions that are repeatable, yet highly configurable and complex.

Management needs to understand how well the HPS infrastructure is functioning, so that decisions about the maintenance and lifecycle of the range infrastructure can be made from the data analytics available. The infrastructure needs to have tools in place to support not only these actions, but the life cycle management of these actions as well. Most importantly, the environment needs to support new tools and processes, and share intellectual property (IP) developed across all levels and users of the environment (administrators, developers, end users, etc.).

BENCHMARK CONFIGURATION FOR EXPERIMENTS

For purposes of showing benchmark and example use cases, we will show two different configurations of infrastructure. One is based on a Dell 2 Node COMET I SDSC 2000 node Dell System which is a high performance simulation stack using an InfiniBand FDR network fabric, Nvidia Tesla V100 GPU Processors (8), SSD PCIe connected to each high end Dell server. The PCIe Network fabric system is based on GigaIO's FabreX technology implementation and is represented by the Rincon (a surfing beach name) system below consisting of a much simpler design using a single PCIe switch connecting all the resources together on a single PCIe tree. Note that significantly lower performing GPUs (GTX1080Ti), NVMe (NonVoltileMemoryExpress), JBoF (JustaBunchofFlash) and single lower end SuperMicro server was used for a much lower cost system (~ $64K) versus the Dell COMET system cost of around $140K. Note that the PCIe Fabric configuration can easily hold more GPUs and JBoF as needed however for these test cases only 8 were used in total. This can be expanded to 64 nodes per the PCIe specification. See Figure 1. Configuration Detail.

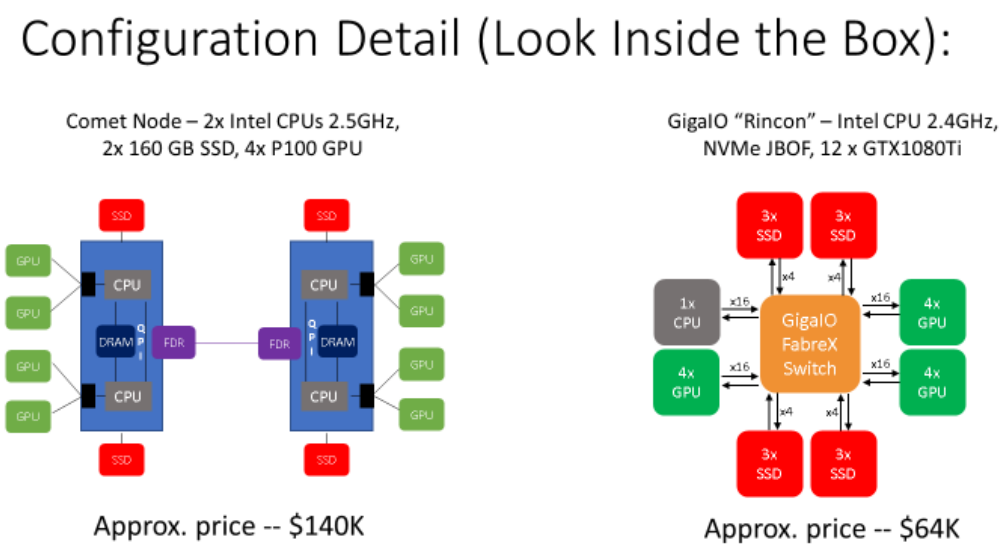

Figure 1. Configuration Detail

BENCHMARK PERFORMANCE DATA USING PCIE NETWORK FABRIC

Using the two configurations above a series of a performance tests were run using some industry standard benchmark suites.

Flexible IO (Fio) is a versatile IO workload generator, widely used as an industry standard benchmark, IO stress testing tool, and for IO verification purposes. GigaIO used this benchmark to test NVMe performance of the GigaIO U.2 Resource Box (JBoF) SSDs connected to the PCIe Bus directly off of a server versus connecting it the FabreX switch. The testing was done across x16, x8 and x4 PCIe Gen3 lanes and based on any combination of Read and Write, sequential or random with any block size, from 4K to 256K, resulted in almost identical performance. See Figure 2. NVMe Performance.

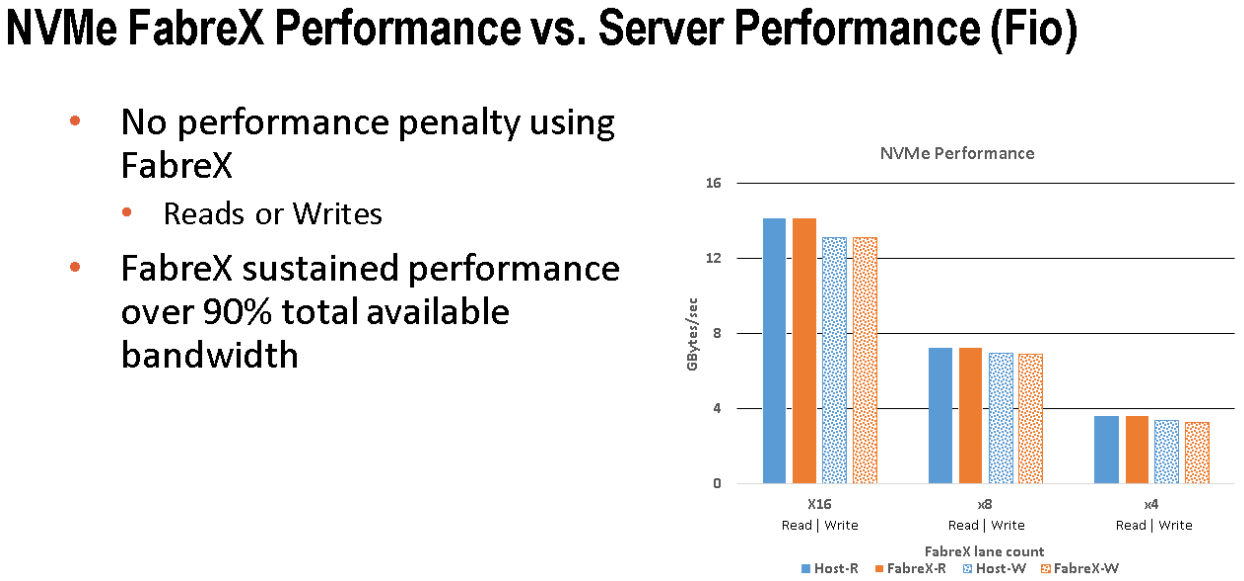

Figure 2. NVMe Performance

Monte Carlo Analysis: a broad class of highly parallel algorithms that rely on repeated random sampling to obtain statistical results used in many scientific and simulation applications showed a favorable iteration time with respect to both strong and weak scalability tests for the FabreX PCIe stack versus the COMET system.

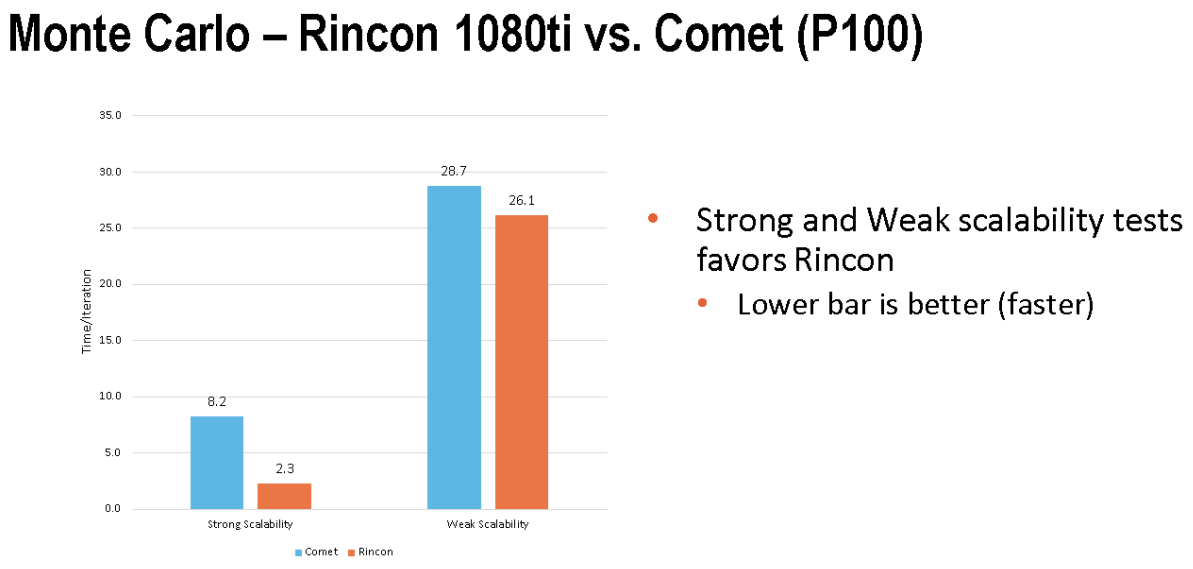

Figure 3. Monte Carlo Performance

EXAMPLE HIGH PERFORMANCE USE CASE WITH PCIE FABRIC

Working with the San Diego Supercomputer Center, the two stacks were used for a typical simulation using the AWP (Anelastic Wave Propagation Simulation) which simulates the dynamic rupture and wave propagation that occurs during an earthquake. This includes a Multi-Terabyte dataset and puts both stacks to the test. As one can see, the FabreX network provides higher performance with much less cost The FabreX stack with 8 GPUs delivers 96%

peak performance compared to 42% for the COMET system. Note the performance of the GPUs at only 1 GPU shows how much more capable the COMET system GPUs are in a direct comparison. Note that at 4 GPUs we are at breakeven in performance and at 8 GPUs the PCIe network fabric results in 50% faster than the Infiniband based COMET implementation. Further addition of more GPUs utilized with a PCIe network fabric would result in even better performance numbers. Note that in order to increase GPU count in the COMET Infiniband implementation additional servers would be required and would drive up cost substantially where the PCIe based environment is more efficient in only the GPUs would be added to the configuration for additional performance. See Figure 4. AWP Performance Results.

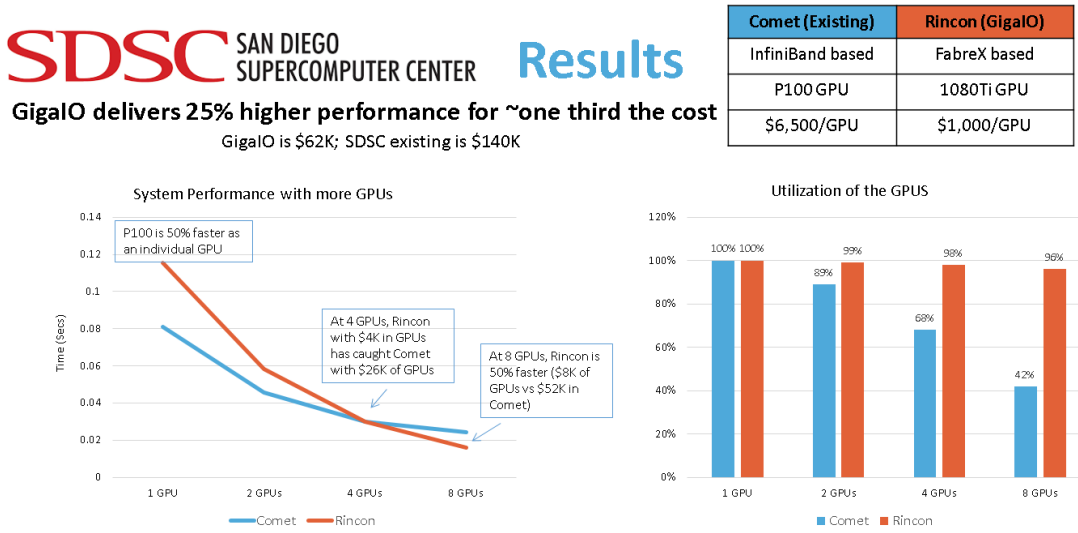

Figure 4. AWP Performance Results

VISUALIZATION PERFORMANCE WITH PCIE FABRIC

An additional benchmark was performed to investigate the visualization ability that a high performance interconnect fabric may be capable of which has implications for graphic intense simulations for DoD simulation and training environments. This was done using the VTK open source visualization tools. See Figure 5. Visualization Setup.

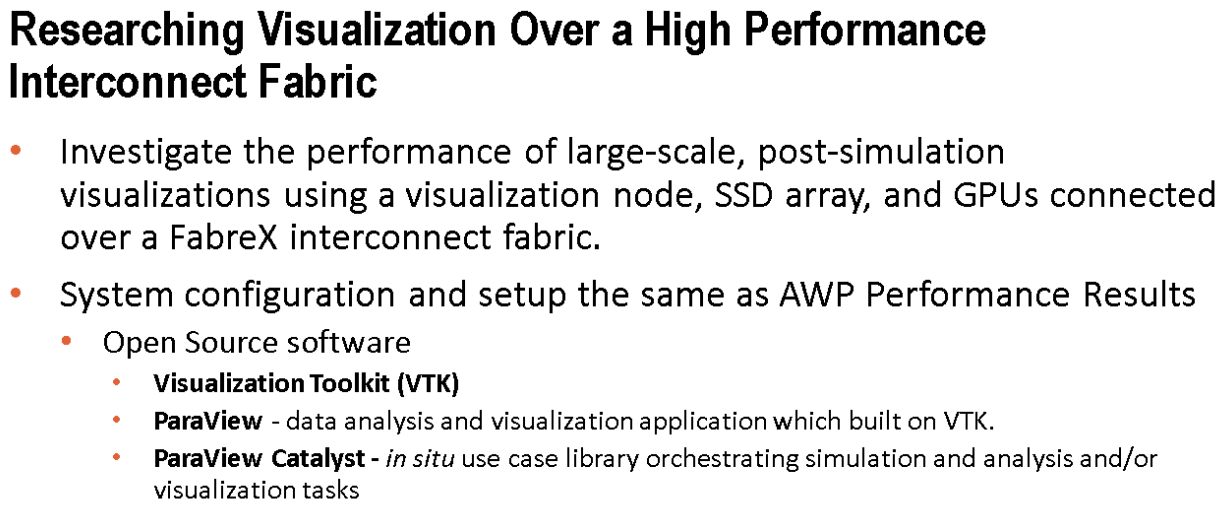

Figure 5. Visualization Setup

Today, numerical simulation plays a vital role in analyzing and assessing earthquakes and their effects. In fact, numerical simulation is used in almost every scientific and technical discipline from structural integrity to bioinformatics to computational fluid dynamics and even on Wall Street. Improvements in computational performance is evident in the exotic high-performance computing architectures, the improvements of storage I/O performance and network bandwidth have not kept pace with the growth of computing power; thus, post-processing has become a bottleneck to end-to-end simulation performance. An approach to solving this performance imbalance is to reduce the amount of output data by implementing in-situ visualization, which constructs the visualization concurrent with the simulation. Beyond restructuring the code to facilitate real-time visualization the system must support a high-bandwidth network. By using the PCIe FabreX network users can offload the computational workload to the GPUs while assigning the visualization workload to the server GPU. The FabreX cluster provides the disaggregation and composability avoiding computational resource waste and boosting the efficiency of the stack.

Note that while this technology has not yet been applied directly to training and simulation requirements, the promise of a much faster visualization can help facilitate the needs of the next generation of 3D and immersive training environments by being able to handle the large data streams that are interacting and being driven by these numerical simulations. The reduction of costs by better utilization and performance of HPC and simulator/training IT resources will no doubt help drive the adoption of new demanding applications in the simulation and training environment. See Figure 6. Visualization Results.

Results -- Visualization in Real-time

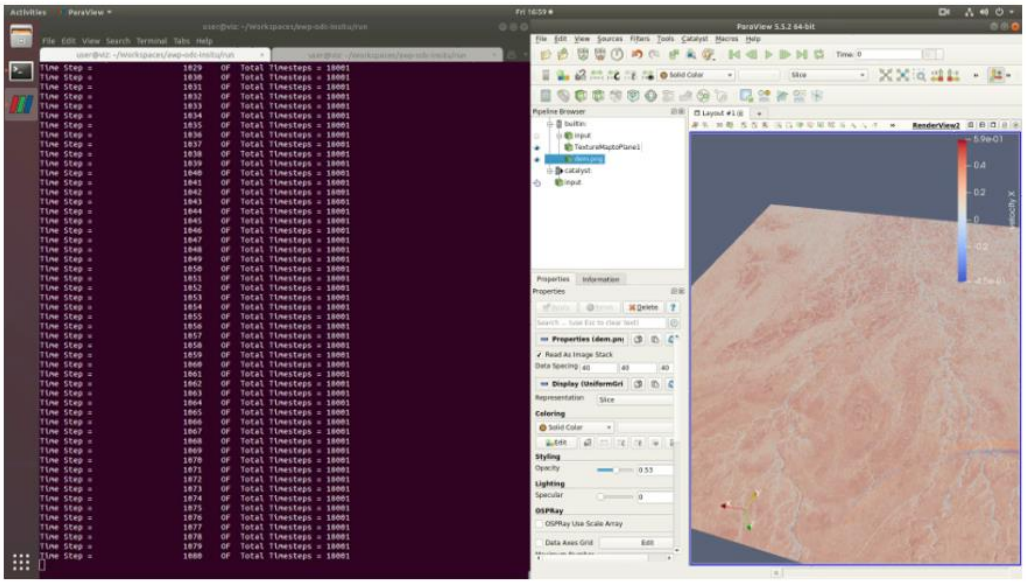

Figure 6. Visualization Results

BENEFICIAL IMPACT OF PCIE FABRIC ON HIGH PERFORMANCE SIMULATION INFRASTRUCTURE

Adoption and deployment of a HPSaaS (High Performance Simulation as a Service) methodology supporting PCIe interconnect network interconnect technology on the HPS environment leads to significant, positive impacts:

Sustainable Auditability
With automation comes built-in documentation of automation processes since the object-oriented method of creating, modifying, and maintaining template elements creates an ongoing and live documentation for process

composition and methodology. Automated equipment maintenance processes with documented schedules provide proof of the compliance of the testing environment. Automated results analysis offers robust reporting that provides solid proof of compliance and compliance efforts. Complete control of all datasets produced by the framework allows for control and ownership of all metrics and outputs produced by the toolset.

A Dramatic Increase In The Velocity Of Infrastructure Delivery.
Organizations (Quali, 2019, p. 1) routinely report time savings upwards of 61% in their deployment cycles once they have automated the process of allocating devices, device/VM provisioning, running automation processes, and generating reports.

Performance
PCIe interconnect network delivers the industry's lowest latency AND the highest effective bandwidth. Latency from system memory of one server to system memory of any other is less than 200ns – true PCIe performance across the entire cluster. The current Gen 3 implementation delivers 256Gbits/sec bandwidth (full duplex), soon to scale up to 512Gbits/sec (full duplex) with PCIe Gen 4. The ability to reconfigure the infrastructure to match the workload further creates efficiency and better use of existing infrastructure resources. This performance will enable further capability for programs such as PCTE, STE and NCRC.

Flexibility

PCIe interconnect network can unite an unprecedented variety of resources, connecting accelerators of all types including GPUs, TPUs, FPGAs and SoCs to other compute elements or storage devices, such as NVMe, PCIe native storage, and other I/O resources. PCIe interconnect network can span multiple servers and racks to scale up single-host systems and scale out multi-host systems, all unified via the PCIe interconnect network software.

Efficiency

Featuring 100% PCI-SIG compliance, the PCIe interconnect network switch can integrate heterogeneous computing, storage and accelerators into one symmetrical system-area cluster fabric, so you can do more with less. Patented technology strips away unnecessary conversion, software layers and overheads that add latency to legacy interconnects.

Significant savings in infrastructure CAPEX and OPEX. Organizations deploying infrastructure automation software report increases of 50% to 200% in device utilization (Quali, 2019, p. 1), leading to capital budget savings, less depreciation waste, as well as accompanying savings in space, power, and cooling costs.

Open Platform, Standards-Based

PCIe interconnect network is built on, and 100% compliant with, the industry's most widely adopted standard, PCI Express, insuring low risk, easy integration and long life. Further, the PCIe interconnect network operating system easily integrates third-party applications with its open-source design, including the DMTF open-source Redfish® APIs to provide unprecedented integration with a range of third-party applications for fabric automation, orchestration, resource allocation and job management.

Memory-Centric Fabric

PCIe interconnect network is the next generation, memory-centric fabric for a changing compute world. Effortlessly connect new memory / storage products, numerous new accelerators and your choice of processors either directly attached or via server configs like NVMe-oF.

Driving Down Cost

The result is lower CAPEX and OPEX through less hardware, higher utilization of resources, lower power consumption, reduced power and less cooling (Acton, Bertoldi, Booth, Flucker, Newcombe, Royer, Tozer, 2018, p. 3). Avoid overprovisioning and add simply the elements you need. Maximize utilization of the footprint of your data center and contribute to your bottom line.

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REFERENCES

Acton, M., Bertoldi, P., Booth, J., Flucker, S., Newcombe, L., Royer, A. and Tozer, R., (2018) Best Practice Guidelines for the EU Code of Conduct on Data Centre Energy Efficiency, *European Commission, Ispra, JRC114148, 3*

Intel (2018) Intel Rack Scale Design Architecture White Paper Data Center, Rack Scale Design *published by Intel,* 1-2

Hoppe, H. & Kenneally, J. editors. (2018) The technology stacks of High Performance Computing and Big Data Computing: What they can learn from each other, *A joint publication between the European associations of www.ETP4HPC.eu and www.BDVA.eu* 15

Lowe, S. (2016) Composable Infrastructure for Dummies, *published by John Wiley & Sons, Inc. Hoboken, NJ, USA, 23-24*

Campbell, S. & Reynolds, C. (2019) Self Service Infrastructure Environment for Next Generation High Performance test and Evaluation (T&E) *The ITEA Journal of Test and Evaluation 2019; 40:* 106-112

Quali (2019) Utilization of Lab Resources Survey Results, *published by Quali*, http://www.quali.com, 1